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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,968	03/31/2004	Kyo-Min Sohn	8021-225 (SS-18860-US)	8696

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EXAMINER	
CAMPOS, YAIMA	
ART UNIT	**PAPER NUMBER**
2185	

DATE MAILED: 04/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/814,968	SOHN ET AL.	
	Examiner	Art Unit	
	Yaima Campos	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 6, 8 and 10-12* is/are rejected.

7)☒ Claim(s) *5,7,9 and 13-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/27/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The instant application having Application No. 10/814,968 has a total of 20 claims pending in the application; there are 2 independent claims and 18 dependent claims, all of which are ready for examination by the examiner.

I. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

II. STATUS OF CLAIM FOR PRIORITY IN THE APPLICATION

As required bye **M.P.E.P. 201.14(c)**, acknowledgement is made of applicant's claim for priority based on applications filed on April 15, 2003 (Republic of Korea – 2003-23733).

III. INFORMATION CONCERNING DRAWINGS

Drawings

3. The applicant's drawings submitted are acceptable for examination purposes.

IV. ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

4. As required by **M.P.E.P. 609(C)**, the applicant's submissions of the Information Disclosure Statement dated May 27, 2005 is acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by

M.P.E.P 609 C(2), a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

V. REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. **Claims 1 and 12** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. As per **claim 1**, the limitations "memory blocks" (line 7) and "data memory blocks" (line 9) render this claim vague and indefinite, as it is not clear to the examiner what is the difference between "memory blocks" and "data memory blocks."

8. As per **claim 12**, it is unclear to the examiner what must be the results of the recited "determinations" in order to "perform a write operation and a read operation;" therefore, claim 12 is considered indefinite.

9. **Claim 12** recites the limitation "the upper address of the read address " in line 16. There is insufficient antecedent basis for this limitation in the claim. The applicants might consider amending this claim to read –**an upper address of the read address** --.

VI. REJECTIONS BASED ON PRIOR ART

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

1. **Claims 1 and 12** are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 14 and 18 of copending Application No. 10/811,613.

2. Initially, it should be noted that the present application and Application No. 10/811,613, have the same inventive entity. The assignee for both applications is Samsung Electronics Co., Ltd..

3. Claimed subject matter in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common

subject matter, as noted below. *See In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993).*

4. Furthermore, there is no apparent reason why applicant would be prevented from presenting claims corresponding to those of the instant application in the other copending application. See MPEP § 804.

5. Claim 1 is compared to claim 14 of application 10/811,613 in the following table:

Instant Application	**Application 10/811,613**
An integrated circuit to which inputs and outputs (I/Os) are separately provided and to which a write address and a read address are simultaneously input during one period of a clock signal, the integrated circuit comprising:	A method of controlling an integrated circuit (IC) to which inputs and outputs (I/Os) are separately provided and to which a write address and a read address are simultaneously input during one period of a clock signal, the method comprising: (claim 1)
a plurality of memory blocks, each of the memory blocks comprising a plurality of sub-memory blocks;	wherein the IC comprises a plurality of the memory blocks, each of the memory blocks comprising a plurality of sub-memory blocks, (claim 13)
a plurality of data memory blocks corresponding to the memory blocks;	determining, a memory block and a data memory block in which a data read operation and a data write operation are to be performed

	in response to the write address and the read address; (claim 1) the data memory blocks corresponding to the memory blocks, (claim 13)
and a tag memory controlling unit, which writes data to the memory blocks or reads data from the memory blocks in response to the write address or the read address, wherein access to the same sub-memory block is not simultaneously performed when the write address and the read address are the same.	and a tag memory controlling unit. (claim 13) wherein the tag memory controlling unit writes data to the memory blocks or reads data from the memory blocks in response to the write address or the read address. (claim 14)

6. Claim 12 is compared to claim 18 of application 10/811,613 in the following table:

Instant Application	**Application 10/811,613**
A method for simultaneously performing a write operation and a read operation in an integrated circuit comprising a separate input and output, the method comprising:	A method for performing a write operation and a read operation in an integrated circuit (IC) comprising a separate input and output (I/O), the method comprising: (claim 15)
determining if a write address and a read address have been input during a period of a	receiving a write address, a read address and a write data command during a period of a clock

clock signal;	signal; (claim 15) determining if the write address and the read address are input; (claim 18)
determining if an upper address of the write address is the same as the upper address of the read address;	determining if an upper address of the write address is coincident with an upper address of the read address; (claim 18)
and performing a write operation and a read operation during the period of the clock signal.	and performing the write operation in one of the first memory location and the second memory location and the read operation in one of the first memory location and the second memory location. (claim 15)

This is a provisional double patenting rejection since the conflicting claims have not yet been patented. The double patenting rejection is also applicable to other claims in the application, for instance, claims 2-11 and 13-20.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. **Claims 1, 6, 8, 10 and 11** are rejected under 35 U.S.C. 102(b) as being anticipated by Bauman (US 6,480,927).

12. As per **claim1**,

"An integrated circuit to which inputs and outputs (I/Os) are separately provided and to which a write address and a read address are simultaneously input during one period of a clock signal, the integrated circuit comprising:" as **[a shared multi-port main memory system having different memory subunits which may perform different memory operations (such as read or write) simultaneously wherein data is transferred in parallel between memory subunits and memory ports (Column 1, lines 27-42 and Column 3, lines 51-24). Bauman also provides an example wherein different memory requests are provided at once during one period of a clock signal (Figure 14A, See lines 1408, 1410, 1412 and 1414 and Column 25, lines 51-54)]**

"a plurality of memory blocks, each of the memory blocks comprising a plurality of sub-memory blocks;" **[With respect to this limitation, Bauman discloses "Memory Storage Unit (MSU)" which contains "storage sub-units called Memory Clusters (MCLs) 535A-535D" (Figure 5 and Column 9, 42-55)]**

"a plurality of data memory blocks corresponding to the memory blocks;" **[With respect to this limitation, Bauman discloses "MDA (Memory Data Crossbar) 530 further includes MSU Data Blocks 720A, 720B, 720C, and 720D, which are interconnected to MCLs (Memory Storage Clusters) 535A, 535B, 535C, and 535D" (Figure 7 and Column 13, lines 56-67)]**

"and a tag memory controlling unit, which writes data to the memory blocks or reads data from the memory blocks in response to the write address or the read address, wherein access to the

same sub-memory block is not simultaneously performed when the write address and the read address are the same" **[Bauman discloses this limitation as "Memory Controller (MCA)" (Figure 5) wherein "MCA 500 provides the control for the POD (Processing Module) Data Blocks 710 and the MSU (Memory Storage Unit) Data Blocks 720" (Column 14, lines 2-11, Figures 5 and 7). Bauman explains that a "Defer Cam" within "memory cluster control block" is used to store addresses associated with "in-progress MSU" operations and when the current address presented for processing coincides with an address entry already stored in the "Defer Cam," then the current address will be added to the "Defer Cam" and the request will be deferred until the "in-progress" operation associated with the same address has been completed (Columns 21-22, lines 53-67 and 1-41, and Figure 12)]**.

13. As per **claim 6**, Bauman discloses "The integrated circuit of claim 1," **[See rejection to claim 1 above]** "wherein the tag memory controlling unit has a same number of decoding addresses as a number of addresses for decoding the data memory blocks" **[With respect to this limitation, Bauman discloses "Address Translate Logic 1130" which "performs a translation function on the address" to map addresses to real memory (Figure 11 and Column 20, lines 13-43). Translation logic must be able to provide the same number of decoding addresses as the number of addresses available in memory]**.

14. As per **claim 8**, Bauman discloses "The integrated circuit of claim 1," **[See rejection to claim 1 above]** "wherein the tag memory controlling unit stores a data memory address indicating that data stored in the data memory blocks is originally data corresponding to one of the sub-memory blocks," **[Bauman discloses this concept as "MSU Data Blocks buffer the data sent to, and received from, the respective MLC. The MCA provide the control"**

(Column 14, lines 1-4, Figure 7) wherein "Directory Array" indicates whether a certain memory unit/block has shared ownership/exclusive ownership of the data (Column 18, lines 38-59)] "and validity determination information for determining whether data stored in the data memory block is valid" **[Bauman discloses this concept as "a directory protocol" wherein "information associated with the status of units of data is stored in memory" (Column 11, lines 6-8 and Column 13, lines 8-22) and also teaches that "a MSU (Memory Storage Unit) is said to have ownership of the data when no other agents have a valid copy of the data" (Column 12, lines 10-17 and Column 14, lines 34-40) as maintaining validity information]**.

15. As per **claim 10**, Bauman discloses "The integrated circuit of claim 1," **[See rejection to claim 1 above]** "wherein the data memory blocks have a direct mapping relation with the sub-memory blocks" **[With respect to this limitation, Bauman discloses "MDA (Memory Data Crossbar) 530 further includes MSU Data Blocks 720A, 720B, 720C, and 720D, which are interconnected to MCLs (Memory Storage Clusters) 535A, 535B, 535C, and 535D" (Figure 7 and Column 13, lines 56-67)]**.

16. As per **claim 11**, Bauman discloses "The integrated circuit of claim 1," **[See rejection to claims 1 above]** "wherein the data is input or output at a single data rate (SDR) or a double data rate (DDR)" **[Bauman discloses this concept as "each MCL (Memory Storage Cluster) includes arrays of Synchronous Dynamic Random Access Memory (SDRAM)" (Column 10, lines 36-37). Note that and SDRAM device is able to transmit data at SDR or DDR]**.

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. **Claims 2-3** are rejected under 35 U.S.C. 103(a) as being unpatentable over Bauman (US 6,480,927) in view of Yoneda (US 5,818,786).

19. As per **claim2**, Bauman discloses "The integrated circuit of claim 1," **[See rejection to claim 1 above]** but does not disclose expressly "wherein the sub-memory blocks are a set of memory cells for sharing a common word line or bit line."

Yoneda discloses the concept of having "memory blocks are a set of memory cells for sharing a common word line or bit line" as **["word lines 47-1, 47-2, ... are respectively extended horizontally through similar memory words 43-1, 43-2, ... of all the memory blocks 42-1, 42-2, ... so that the same main word signal is applied from the main decoder 45 thereto. On the other hand, memory block selection lines 48-1, 48-2, ... are vertically extended so that different block selection signals are supplied from the subdecoders 46-1, 46-2, ... to all the memory words 43-1, 43-2, ... of the respective memory blocks 42-1, 42-2 ...." (Figure 1 and Column 12, lines 44-54)]**.

Bauman (US 6,480,927) and Yoneda (US 5,818,786) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the integrated circuit to which inputs and outputs are separately provided and to which a read and a write address are simultaneously input as taught by Bauman and further have memory blocks sharing a common word line or bit line as taught by Yoneda.

The motivation for doing so would have been because Yoneda discloses that having memory blocks sharing a common word line or bit line makes it possible to have **["high speed operation" as "signal speed on the main word line is increased" (Column 9, lines 29-58)]**.

Therefore, it would have been obvious to combine Yoneda (US 5,818,786) with Bauman (US 6,480,927) for the benefit of creating an integrated circuit capable of simultaneously performing data read and data write operations to obtain the invention as specified in claim 2.

20. As per **claim 3**, Bauman disclose "The integrated circuit of claim 1," **[See rejection to claim 1 above]** but fails to disclose expressly "sub-memory blocks," wherein "two or more word lines or bit lines cannot be simultaneously activated."

Yoneda discloses the concept of "sub-memory blocks," wherein "two or more word lines or bit lines cannot be simultaneously activated" as it is taught that **["the bit line structure of the memory cell differs depending on whether or not the two subword lines are simultaneously made active" (Column 13, lines 3-5) and explains that "one set of bit lines for common use is sufficient in a case where these subword lines are not activated simultaneously" (Columns 13-14, lines 63-67 and 1-8)]**.

Bauman (US 6,480,927) and Yoneda (US 5,818,786) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the integrated circuit to which inputs and outputs are separately provided and to which a read and a write address are simultaneously input as taught by Bauman and further provide a memory block where two or more bit lines are not simultaneously activated as taught by Yoneda.

The motivation for doing so would have been because Yoneda discloses that providing a memory block where two or more bit lines are not simultaneously activated makes it possible to **[access word lines independently and for example, allows for providing "access independently to even- or odd-numbered bits of the memory word" (Column 11, lines 23-28)]**.

Therefore, it would have been obvious to combine Yoneda (US 5,818,786) with Bauman (US 6,480,927) for the benefit of creating an integrated circuit capable of simultaneously performing data read and data write operations to obtain the invention as specified in claim 3.

21. **Claims 4 and 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Bauman (US 6,480,927) in view of Kim et al. (US 2004/0085817).

22. As per **claim 4**, Bauman discloses "The integrated circuit of claim 1," **[See rejection to claim 1 above]** but does not disclose expressly that a "data memory blocks has the same size as one sub-memory block."

Kim discloses, a "data memory blocks" having "the same size as one sub-memory block" as **[a first in/first out multi-port memory having an improved input/output method wherein a memory block is subdivided into N memories and read/write transactions are performed**

simultaneously (Figure 3 memory block 100 and memories 110 and 120 which have the same size and Column 2, paragraph 0036)].

Bauman (US 6,480,927) and Kim et al. (US 2004/0085817) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the integrated circuit to which inputs and outputs are separately provided and to which a read and a write address are simultaneously input as taught by Bauman and further provide data memory blocks and sub-memory blocks having the same size, as taught by Kim.

The motivation for doing so would have been because Kim discloses that providing data memory blocks and sub-memory blocks having the same size makes it possible to **[obtain faster speed as having a 2 memories within a block provides fast-speed for input/output, but having N number of memories within a memory block would increase input/output speed by N times (Column 4, paragraph 0055)].**

Therefore, it would have been obvious to combine Kim et al. (US 2004/0085817) with Bauman (US 6,480,927) for the benefit of creating an integrated circuit capable of simultaneously performing data read and data write operations to obtain the invention as specified in claim 4.

23. As per **claim 12**, Bauman discloses

"A method for simultaneously performing a write operation and a read operation in an integrated circuit comprising a separate input and output, the method comprising:" **[a shared multi-port main memory system having different memory subunits which may perform different memory operations (such as read or write) simultaneously wherein data is transferred in**

parallel between memory subunits and memory ports (Column 1, lines 27-42 and Column 3, lines 51-24)]

"determining if a write address and a read address have been input during a period of a clock signal;" **[Bauman also provides an example wherein different memory requests are provided at once during one period of a clock signal (Figure 14A, See lines 1408, 1410, 1412 and 1414 and Column 25, lines 51-54)]**

"determining if an upper address of the write address is the same as the upper address of the read address;" **[Bauman discloses this limitation as "Memory Controller (MCA)" (Figure 5) wherein "MCA 500 provides the control for the POD (Processing Module) Data Blocks 710 and the MSU (Memory Storage Unit) Data Blocks 720" (Column 14, lines 2-11, Figures 5 and 7). Bauman explains that a "Defer Cam" within "memory cluster control block" is used to store addresses associated with "in-progress MSU" operations and when the current address presented for processing coincides with an address entry already stored in the "Defer Cam," (*Therefore, it is determined whether the address of a current operation coincides with the address of an in-progress operation*) then the current address will be added to the "Defer Cam" and the request will be deferred until the "in-progress" operation associated with the same address has been completed (Columns 21-22, lines 53-67 and 1-41, and Figure 12)]**.

Bauman does not expressly disclose "performing a write operation and a read operation during the period of the clock signal."

Kim discloses "performing a write operation and a read operation during the period of the clock signal" as **["first-in first-out memory circuit using a standard cell library memory,**

including: a memory block having N number of memories (N>1); a read pointer for designating read addresses of the N number of memories; a write pointer for designating write addresses of the N number of memories; and a memory controller for selecting one from the N number of memories based on the read/write addresses, generating n number or read/write clock signals by demultiplying a clock signal by n (n=N, n>1) and sending the n number of read/write clock signals having a 1/n cycle difference to the N number of memories thereby inputting/outputting data" (Column 2, paragraph 0022)].

Bauman (US 6,480,927) and Kim et al. (US 2004/0085817) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the integrated circuit to which inputs and outputs are separately provided and to which a read and a write address are simultaneously input as taught by Bauman and further perform a read/write operation within one period of a clock signal, as taught by Kim.

The motivation for doing so would have been because Kim discloses that performing a read/write operation within one period of a clock signal makes it possible to **[obtain synchronization during memory input and output processing (Column 4, paragraphs 0023, 0038 and 0057)]**.

Therefore, it would have been obvious to combine Kim et al. (US 2004/0085817) with Bauman (US 6,480,927) for the benefit of creating an integrated circuit capable of simultaneously performing data read and data write operations to obtain the invention as specified in claim 12.

VII. RELEVANT ART CITED BY THE EXAMINER

24. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

25. The following reference teaches an n-dimensional multi-port memory in which a memory circuit is divided into upper and lower memory blocks.

U.S. PATENT NUMBER

US 5,303,200

26. The following reference teaches a semiconductor memory device in which inputs/outputs are synchronized with a clock signal.

U.S. PATENT NUMBER

US 6,356,484

27. The following reference teaches a simultaneous access to multiple memories by multiple ports.

U.S. PATENT NUMBER

US 5,226,010

VIII. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

28. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) SUBJECT MATTER CONSIDERED ALLOWABLE

29. Per the instant office action, claims 5, 7, 9 and 13-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The primary reasons for allowance of claim 5 in the instant application is the combination with the inclusion in this claim of the limitation of an integrated circuit to which inputs and outputs are separately provided and to which a read and a write address are simultaneously input wherein "**if each of the data memory blocks has the same size as one sub-memory block, the data memory blocks have a number of columns and rows different from a number of columns and rows of the sub-memory block.**" The prior art of record including the disclosures under section **VII** above neither anticipates nor renders obvious the above recited combination.

The primary reasons for allowance of claim 7 in the instant application is the combination with the inclusion in this claim of the limitation of an integrated circuit to which inputs and outputs are separately provided and to which a read and a write address are simultaneously input wherein "**the tag memory controlling unit has a number of columns and rows different from a number of columns and rows of the data memory blocks.**" The prior art of record including the disclosures under section **VII** above neither anticipates nor renders obvious the above recited combination.

The primary reasons for allowance of claims 9 in the instant application is the combination with the inclusion in this claim of the limitation of an integrated circuit to which inputs and outputs are separately provided and to which a read and a write address are simultaneously input wherein **"if the number of the sub-memory blocks is 2N, each address**

of the tag memory controlling unit includes N+1 data bits, and N-bit of the N+1 data bits indicates a data memory address, and remaining 1-bit of the N+1 data bits indicates the validity determination information." The prior art of record including the disclosures under section **VII** above neither anticipates nor renders obvious the above recited combination.

The primary reasons for allowance of claims 13-20 in the instant application is the combination with the inclusion in this claim of the limitation of an integrated circuit to which inputs and outputs are separately provided and to which a read and a write address are simultaneously input wherein **determining if the write address and the read address are the same as a data memory address, when it is determined that the upper address of the write address and the upper address of the read address are the same** and **determining if the write address and the read address are coincident with a data memory address, when it is determined that the upper address of the write address and the upper address of the read address are not the same**.. The prior art of record including the disclosures under section **VII** above neither anticipates nor renders obvious the above recited combination.

a(2) CLAIMS REJECTED IN THE APPLICATION

30. Per the instant office action, claims 1-4, 6, 8, and 10-12 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232. The examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

IMPORTANT NOTE

32. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Donald Sparks, can be reached at the following telephone number: Area Code (571) 272-4201.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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